PhD Dissertation Defense Announcement
Mechanical and Aerospace Engineering Department
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RELIABILITY ENHANCEMENT OF HETEROGENEOUS 3D INTEGRATED CIRCUIT AND CHARACTERIZATION OF THERMAL INTERFACE MATERIAL

By

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1:30 PM, Thursday, July 30, 2020

Microsoft Teams Link

Abstract

Consumer electronic products such as digital cameras, cellphones etc. requires high fictional integration in small footprints with lower cost. This requires that effective communication be maintained between the IC's and the electronic systems without compromising with the cost and form factor owing to the increased complexity. Hence, the various challenges arising due to the factors like signal processing time, heat dissipation, structural integrity, chip package interaction such issues need to be dealt effectively during electronic packaging. 3D stacking of the processors and the components accomplishes the goals and in high computing application it reduces the delay. 3D TSV technology is the heart of 3D integration and stacking of dies. Generally, in a TSV package, a thin silicon wafer is drilled with through holes, and dielectric SiO_2 is deposited along the inside walls of the holes, and then the hole is filled with Copper. Since the TSV's go through dice, and dice have transistors, the transistors cannot be placed in a thermally stressed area, since it will not function in that area. It is challenging to remove heat from the dice which are stacked. Due to the heat, we have thermal stresses developed at the interfaces of different materials, which causes structural integrity issues like cracking and warpage. Different materials try to expand and compress according CTE values. Also, the interface of silicon/silicon dioxide is brittle and hence crack can form at the Cu TSV and Si/SiO_2 interface. This study focuses on analysis of structural integrity during die attachment process of a 2-die 3D TSV package to gauge the Stress Intensity

Factors in TSV/Silicon interface thereby highlighting the prevalent modes of cracking in TSV. Another part of the study deals with the effects of the die thickness on the stress intensity factor arising in the TSV with respect to design changes and J-Integral values are studied with respect to different crack positions on TSV.

Heat dissipation of the semiconductor packages has become one of the limiting factors in miniaturization. Thermal interface material plays a significant role in the electronic devices for transferring heat since it enhances the heat transfer rate between contact surfaces. It is one of the most important materials that is used in an electronic package. When two solid surfaces are attached there can be microvoids between the surfaces. These voids are generally filled by air, which increases the thermal resistance. Without good thermal contact heat dissipating devices cannot dissipate heat efficiently. For good thermal contact thermal interface materials are required. Characterization of the properties of thermal interface materials has gained importance since it plays a critical role in the thermal dissipation and the life cycle of the of the electronic packages. In this study silicone and silicone-free thermal interface materials are studied. Properties such as modulus of elasticity, coefficient of thermal expansion, and dielectric properties are studied, and effect of silicon content is investigated. The effect of thermal aging on the properties of silicone and silicone-free thermal interface materials are also analyzed in this study.