Master's Thesis Defense Announcement
Mechanical and Aerospace Engineering Department
University of Texas at Arlington

Structural Optimization and Reliability Assessment of Heterogeneous 3D IC Packages and Analysis of Rheological Properties of Particle Based Thermal Interface Material

By
Mehzabeen Binte Kabir

Thesis Advisor: Professor Dereje Agonafer

1:00 PM, Tuesday, March 23, 2021

Microsoft Teams

https://teams.microsoft.com/l/meetup-join/19%3ameeting_YjMwNGEwNDAtN2Y2NC00ZmY0LThiMjAtYmI5YmJiMDA4NTZi%40thread.v2/0?context=%7b%22Tid%22%3a%225cdc5b43-d7be-4caa-8173-729e3b0a62d9%22%2c%22Oid%22%3a%22d4c59367-41bb-4f4b-8b23-50692ad45d16%22%7d

Abstract

As computing and communication devices are converging with improved functionally, denser, and finer pitch which creates complexity of circuit interconnections for 2-D devices becomes a limitation for performance and drives up power dissipation. Thus the ordinary 2-D structures of IC packages cannot address those demands where 3-D through-silicon via (TSV) is the key to 3-D IC integration and stacking of chips, is emerging now as a powerful tool to converge the needs of integrated circuit (IC) packages. In 3D TSV the chips are stacked on top of another so heat trapped in a small region which is difficult to dissipate that may cause failures in electronic devices. Also, the high CTE mismatch between low-k dielectric layer and the copper core is one of the critical challenges for 3-D IC packages. In this study, the effect of the optimization of the structure of a 2-die flip chip BGA package has been studied. Stress intensity factor, which indicates the state of stress near a crack tip and J-integral values are used to specify the crack driving force have been analyzed with the change of die thickness at different positions on TSV. Varying the thickness of die the crack is modeled on TSV which is studied during the chip attachment process. Finite element analysis (FEA) is used to examine the thermo-mechanical stresses and fracture parameters of the 3D IC package. Under Reflow condition and Thermal Cycling condition the optimization of the structure of the chips are taken place to analyze the reliability assessment of the package. The materials used for TSV and solder bumps are another important factor which impact package reliability. Comparisons of material properties of the copper core of TSV are studied to show how it can affect the package reliability.

In today's digitalized industries one of the most critical challenge is thermal management of the electronic devices with improved functionality. As heat dissipation is very crucial thermal interface materials (TIMs) plays a vital role for dissipating heat of electronic devices. Particle laden thermal interface materials are one of the most widely used TIMs in microprocessor cooling solutions. Thermal conductivity of such particle laden TIMs increases with the volume fraction of conductive particles added to the thermal interface materials. These volume fraction of conductive particles not only affects the thermal conductivity of thermal interface materials but also impacts the bond line thickness (BLT) and other rheological properties such as viscosity and shear modulus of TIMs after a certain limit. The uniformity of particle laden TIMs to cover the interfaces of the components of electronic packages depend on the viscosity of such materials. In this analysis two types of micro particle based TIMs, TIM A and TIM B are used to measure the change of viscosity at room temperature using Discovery Hybrid Rheometer (HR-2) at different gap between two parallel plates of the rheometer to see how the viscosity of these TIMs changed with confinement and reach to a constant value with the change of shear rate. It is crucial to measure the rheological properties of such particle laden thermal interface materials as it is related to the thermal conductivity of TIMs and can enhance thermal management or heat dissipation of electronic devices.