PhD Dissertation Defense Announcement
Mechanical and Aerospace Engineering Department
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Reliability assessment of Cu-Cu hybrid bonded advanced heterogenous 3D integrated circuits and Impact of signal phase immersion cooling on electronics package

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Abstract

Detailed study of material compatibility of the various electronics packaging materials for immersion cooling is essential to understand their failure modes and reliability. The modulus and thermal expansion are critical material properties for electronics mechanical design. Substrate is a critical component of electronic package and heavily influences failure mechanism and reliability of electronics both at the package and board level. This study mainly focuses on two major challenges. The first part of the study focuses on the impact of thermal aging in dielectric fluid for single-phase immersion cooling on the non-halogenate substrate's thermo-mechanical properties. The second part of the study is the impact of thermal aging on thermo-mechanical properties of substrate in the air. The non-halogenated low Coefficient of Thermal Expansion (CTE) bismaleimide triazine (BT) resin laminate is used for its ultra-low CTE which in turn reduce the warpage of substrate. Moreover, the substrate has high glass transition temperature and high stiffness suitable for the application which requires high heat resistance. The substrate is aged in ElectroCool EC100 dielectric fluid, and air for 720 hours at three different temperatures: 22°C, 50°C, and 75°C. The complex modulus is characterized before and after aging for both parts and compared. Moreover additional 3 PCBs samples and 3 substrates samples aged in 3 different immersion fluids were characterized and compared to draw the relationship between the glass transition temperature of the material and the impact of immersion on the thermo-mechanical properties.

Bump-less direct Cu-Cu hybrid bonding interconnection technology helps achieve high-density and fine-pitch applications such as high-performance computing. It provides much lower electrical resistivity and lower electromigration compared to C4 (controlled collapse chip connection) solder bumped flip assembly and C2 (chip connection, micro-bump, or Cu-pillar with solder cap) bumped flip chip assembly. In this study, multi-level sub-modeling approach is utilized to study the bump-less Cu-Cu bonded interconnect reliability of the 3D TSV package during Cu-Cu thermal compression bonding (TCB) process. Most direct Cu-Cu TCBs requires diffusion of Cu atoms across the interface to form monolithic copper at high temperature (350 – 400°C). Fracture mechanics parameters was calculated at Cu-Cu bonded region, Si/TSV region and back-end Cu/dielectric stack under TCB thermal loads. Further, multivariable design optimization is carried out to improve the reliability of advanced interconnects.