PhD Dissertation Defense Announcement
Mechanical and Aerospace Engineering Department
University of Texas at Arlington

Reliability assessment of 2.5D Heterogenous Integrated Circuits, Cu-Cu Hybrid Bonded Interconnects and Thermo-mechanical Assessment of Substrates in Two-Phase Immersion Cooling

By : Akshay Lakshminarayana
Thesis Advisor: Dereje Agonafer
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Abstract

Moore's law has predicted the growth of semiconductor industry for the last 50 years by providing a template for silicon scaling and homogenous system on chip integration of multiple circuits. Lately, this trend has been declining due to the increased power density and functionality and increasing chip size to accommodate this. Moving forward, heterogeneous integration of chiplets will improve the silicon yield by integrating multiple multi-functional chiplets that are of smaller area onto an interposer or a substrate in 2.5D, 3D or 3.5 D architectures. In this study, computational analysis is done on the impact of design parameters and material properties on the reliability of a quarter-symmetric model of a 2.5D package with an ASIC (Application Specific Integrated Circuit) and 4 HBM (High Band-width Memory) modules around integrated through an interposer. JEDEC standard loading of thermal cycling loads are applied on the package to emulate long term thermal loads that the package is subjected to. -40C to 125C at a ramp time of 300 sec and dwell time of 1800 seconds is applied to the entire package. All three different kinds of interposers namely Si, glass and organic interposers are evaluated for their impact on the total deformation, Von-Moises stress on the solders, die and the substrate.

Bump-less direct Cu-Cu hybrid bonding interconnection technology helps achieve high-density and fine-pitch applications such as high-performance computing. It provides much lower electrical resistivity and lower electromigration compared to C4 (controlled collapse chip connection) solder bumped flip assembly and C2 (chip connection, micro-bump, or Cu-pillar with solder cap) bumped flip chip assembly. In this study, multi-level submodeling approach is utilized to study the bump-less Cu-Cu bonded interconnect reliability of the 2.5D TSV package during Cu-Cu thermal compression bonding (TCB) process. Most direct Cu-Cu TCBs requires diffusion of Cu atoms across the interface to form monolithic copper at high temperature (350 – 400°C). Fracture mechanics parameters was calculated at Cu-Cu bonded region, Si/TSV region and back-end Cu/dielectric stack under TCB thermal loads. Further, multivariable design optimization is carried out to improve the reliability of advanced interconnects.

Detailed study of material compatibility of the various electronics packaging materials for immersion cooling is essential to understand their failure modes and reliability. The modulus and thermal expansion are critical material properties for electronics mechanical design. Substrate is a critical component of electronic package and heavily influences failure mechanism and reliability of electronics. The non-halogenated low Coefficient of Thermal Expansion (CTE) bismaleimide triazine (BT) resin laminate is used for its ultra-low CTE in high frequency applications which in turn reduce the warpage of substrate. Moreover, the substrate has high glass transition temperature and high stiffness suitable for the application which requires high heat resistance. The substrate is aged in a two-phase dielectric fluid, and air for 720 hours at room temperature and 45°C (just below its boiling point). The complex modulus is characterized before and after aging for all kinds of substrates and compared to draw the relationship between the modulus of the material and the impact of immersion on the thermo-mechanical properties.